Software-Driven Optimization for Performance, Power, and Thermal Tradeoffs

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ABSTRACT

Software development continues to cause profound changes for design of electronic components. Hardware-software optimizations for power, performance and area have been known trade-offs in the past, now thermal effects are adding additional complexity to the set of options to be considered. To enable as accurate power estimation as possible, the effects of the semiconductor implementation captures in .lib files increasingly need to be connected to dynamic effects as well as the software executing on processors on the system on chip (SoC), captured in switching information, for example represented in SAIF files. Thermal effects may become visible only after sufficient run-time of the software in the design, with for example AnTuTu benchmarks dropping when adding more processors that eventually have to be throttled.

This presentation will illustrate a methodology for dynamic power analysis, linking software executing in emulation on the processors of a SoC all the way to TSMC technology representations. We will introduce different types of toggle formats, allowing the efficient selection of a time-window of interest to be analyzed further. With fully accurate toggle formats users then can dive into more detail, feed them into logic synthesis, allowing to annotate power estimates back into the analysis of software as well as the dynamic behavior as executed in emulation.

As examples we will introduce case studies in which users were able to achieve greater than 90% accuracy compared to the actual dynamic power consumption of the SoCs. We will close with a preview of approaches how to even more closely connect TSMCs technology into the front-end of functional verification and software development.

Software-Driven Optimization for Performance, Power, and Thermal Tradeoffs

Frank Schirrmeister and T.C. Lin
TSMC OIP Ecosystem Forum
San Jose, CA
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Agenda

- Low power as part of metric-driven signoff
- Dynamic power analysis
  - Deep cycles
  - Types of toggle counts
  - RTL and gate-level dynamic power analysis
  - Texas Instruments example
- Summary

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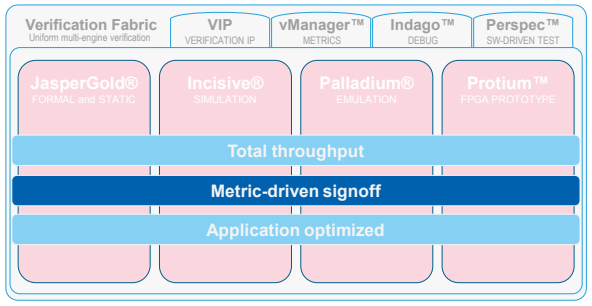
Low Power as Part of Metric-Driven Signoff



- Best-in-class engines
- Flow-driven engine integrations
- **Differentiated and comprehensive solutions**

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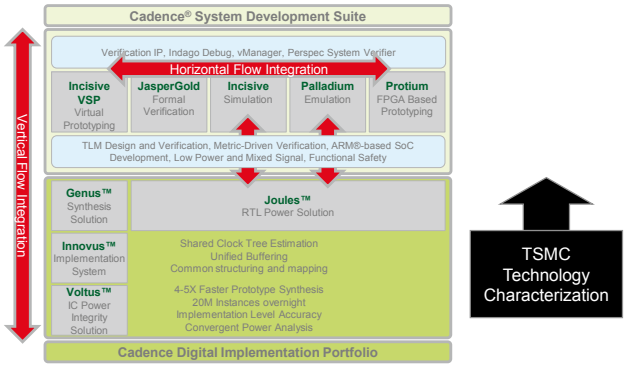
Horizontal and Vertical Flow Integration



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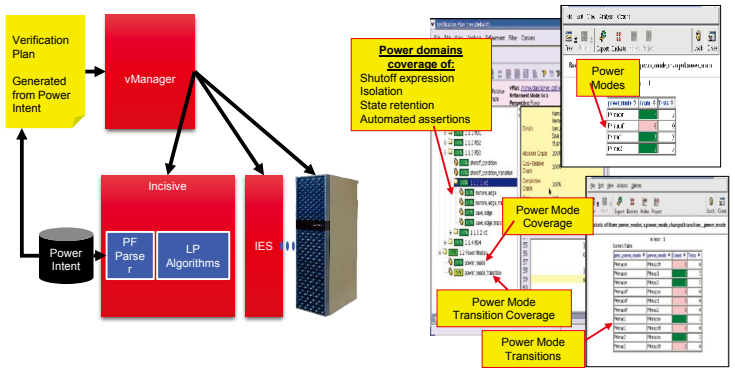
Metric-Driven Native Power-Aware Verification

Plan, execute, monitor, and track progress of low-power verification



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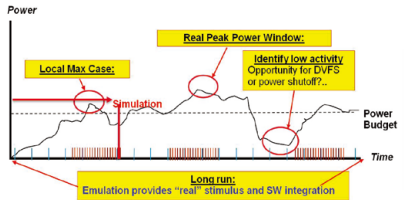
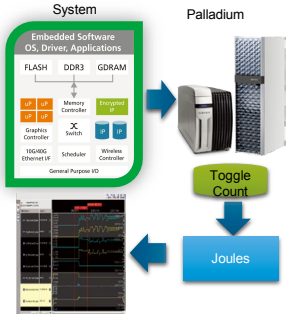
Dynamic Power Analysis

High-throughput, system-level power estimation





- Uncovering power issues may require thousands to billions of cycles
- Palladium platform runs real-world scenarios and identifies peak power issues early
- Incisive simulator provides greater visibility in selected windows

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Dynamic Power Analysis

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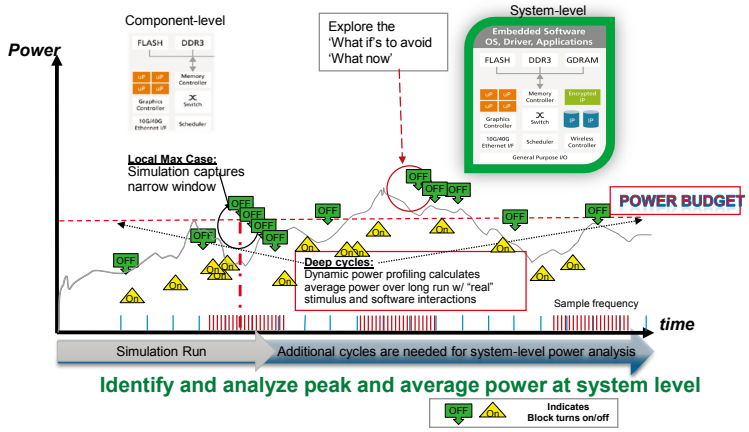
SoC Power Analysis Requires "Deep" Cycles

@100MHz for 10 secs → 1 billion cycles



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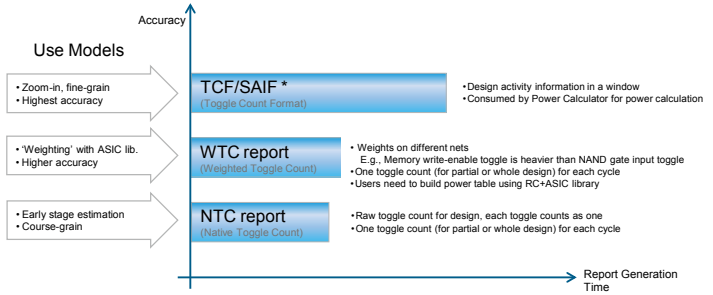
Three DPA Reports—NTC, WTC, TCF/SAIF
Flexible use models



* Shown here is the relative time to generate TCF file compared to WTC or NTC. Additional analysis time required to run through power calculator

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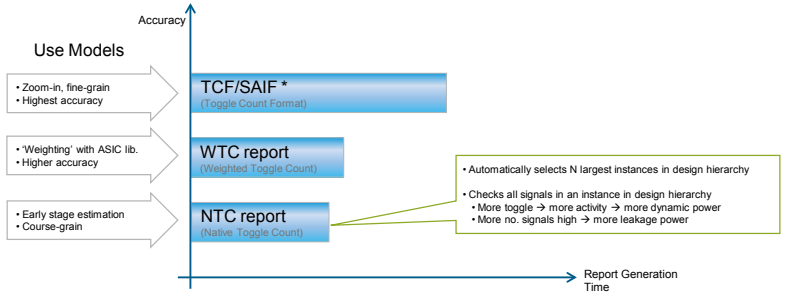
Three DPA Reports—NTC, WTC, TCF/SAIF
Flexible use models



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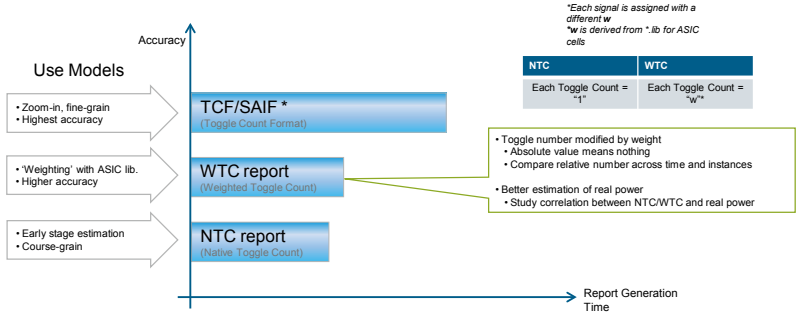

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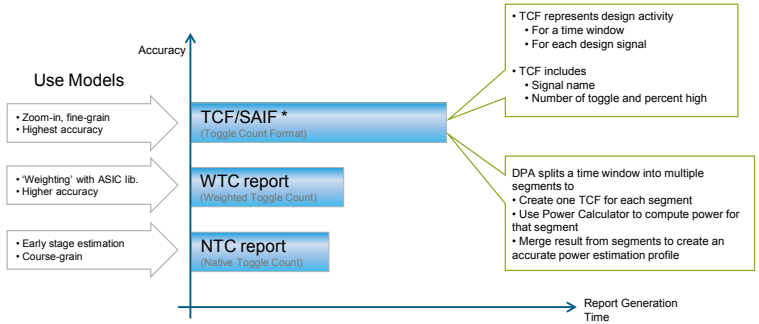

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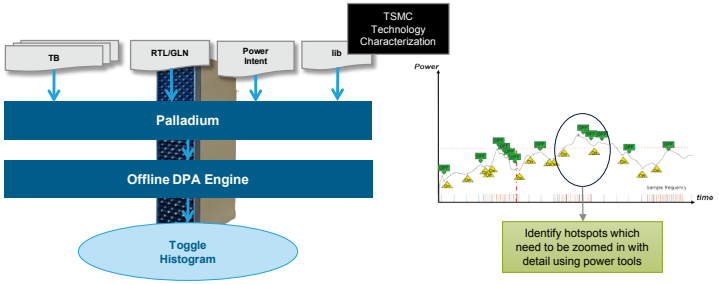
Dynamic Power Analysis (DPA)

Use mode 1—Compute initial power trends



- Generate native and weighted toggle count reports for coarse-grain power estimation
- Identify early architectural issues

*DPA is a licensed option

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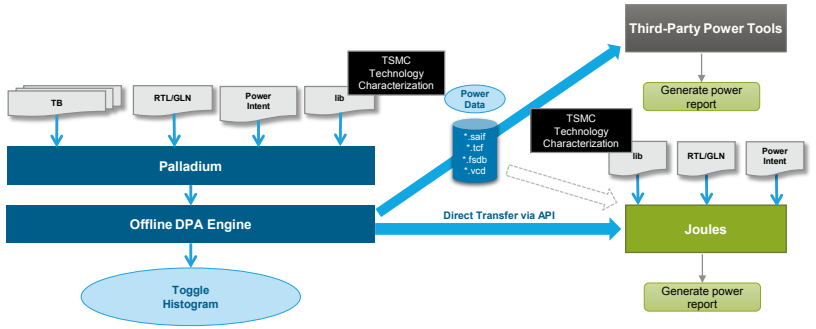
Dynamic Power Analysis (DPA)

Use mode 2—Generate detailed power reports



Fast and accurate RTL/gate-level power analysis for thorough hardware-software verification

*DPA is a licensed option

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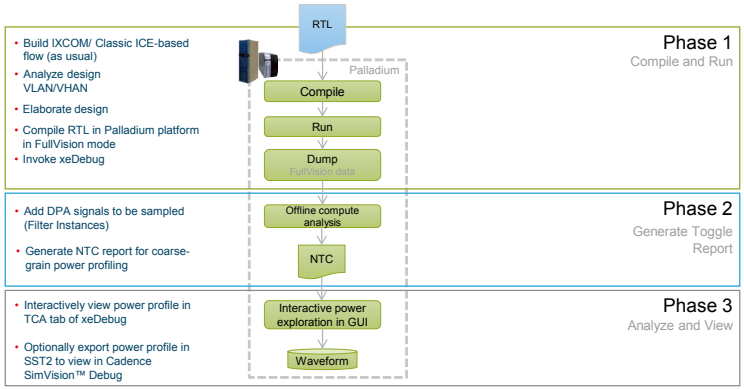
RTL Dynamic Power Analysis

NTC (Native) flow, based on toggle count



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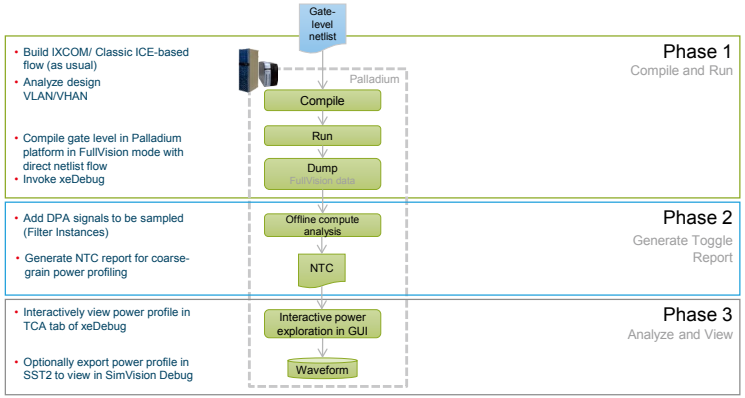
Gate-Level Dynamic Power Analysis

NTC (Native) flow, based on toggle count



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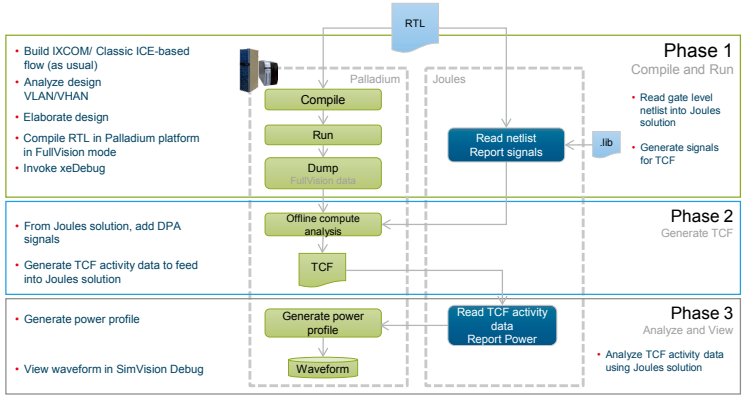
RTL Dynamic Power Analysis

TCF-based flow with Joules RTL Power Solution



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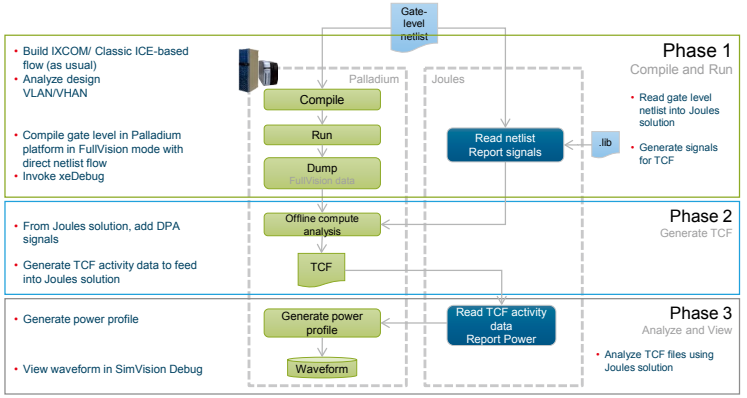
Gate-Level Dynamic Power Analysis

TCF-based flow with Joules RTL Power Solution



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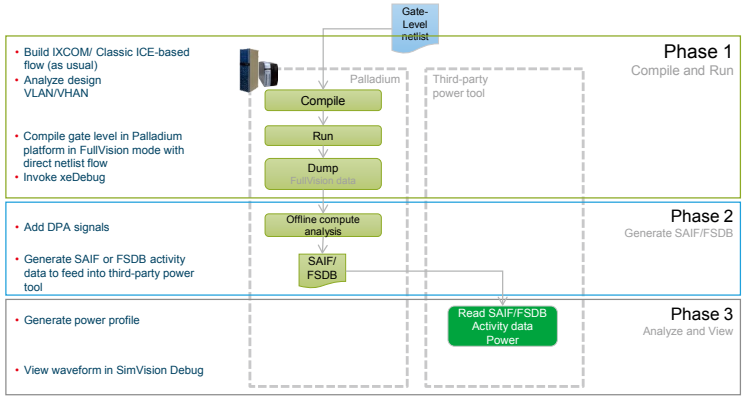
Gate-Level Dynamic Power Analysis

SAIF/FSDB-based flow with third-party power tool



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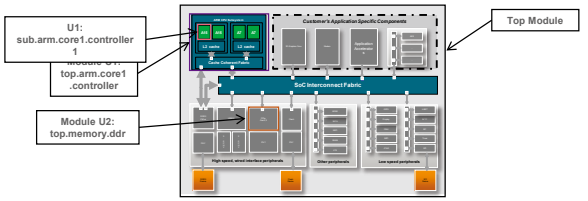
Performance—Module/Instance-Based FullVision

- Compute FullVision specific design module or instance instead of whole design
- DPA data can be extracted from chosen module compiled with FullVision
- Re-compile and re-run for DPA data of additional modules
  - Try to choose a design module which covers most module/instance of interest



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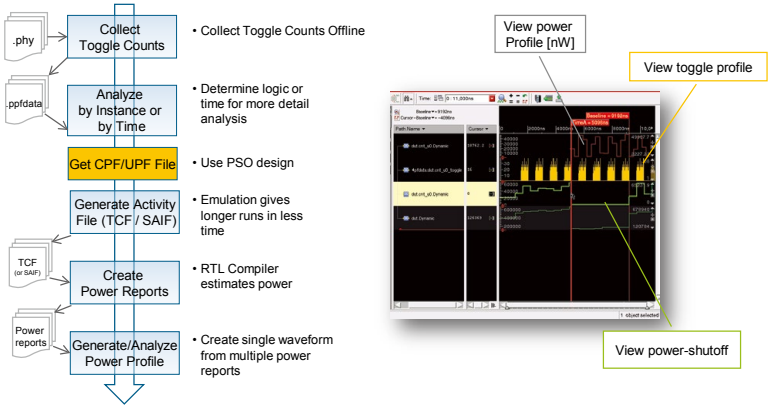
Integrate Low-Power Design with Dynamic Power Analysis



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DPA Success Story: Texas Instruments

- Business challenges
  - Deliver the best application processor with optimal performance, power consumption, and thermal conditions
  - Limit power consumption within two watts
- Design challenges
  - Provide accurate power estimation based on real use cases
  - Develop a methodology, power dashboard, and continually track power updates
  - Achieve close correlation between an architect's power estimation and actual silicon measurement
- Cadence solutions
  - Palladium Dynamic Power Analysis
  - Encounter® Power System
- Results
  - Power estimation and actual silicon measurement at 96% accuracy
  - Detected unexpected power peaks and resolved design to lower power consumption

http://www.cadence.com/rl/Resources/success_stories/ti2_cs.pdf

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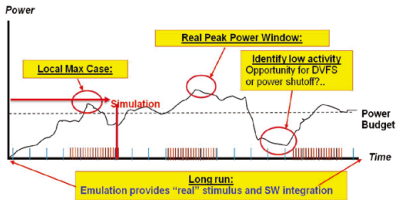
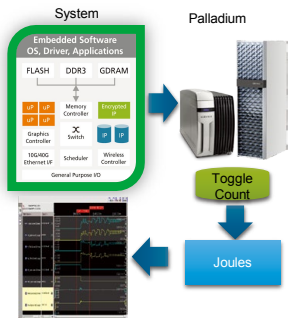
Dynamic Power Analysis

High-throughput, system-level power estimation





- Uncovering power issues may require thousands to billions of cycles
- Palladium platform runs real-world scenarios and identifies peak power issues early
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Metric-driven signoff

Quality via multi-engine metrics aggregated in vManager, from IP to SoC level

- Code **coverage**
- **Assertions**
- **IP** integration
- **Mixed signal** integration

Design quality

- **Power** management
- Interconnect **performance**
- **Protocol** compliance
- Requirement **traceability**

System quality

- Web-based **dashboard**
- Automated rollup
- Identify and close gaps

Management visibility

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